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| 10/038,742 | 12/31/2001 | Sushma Shrikant Trivedi | 4860.P2691 | 3350 |

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James C. Scheller
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

| EXAMINER | |
|---|---|
| PAN, DANIEL H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/038,742 | TRIVEDI ET AL. | |
| | Examiner | Art Unit | |
| | Daniel Pan | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/31/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-71 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-13,19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beard (5,430,884) in view of So (5,909,559).

3. Beard taught at least :

a) host (not explicitly shown) and a host memory (see the main memory in fig.1, see also fig.17)

b) a chip interconnect (44, see fig.1, fig.17, see comment below) ;

c) a memory controller (see the address mechanism and the arbitration node in fig.17) for controlling the host memory coupled to the chip interconnect',

d) a scalar processing unit [102] coupled to the chip interconnect [44], the scalar processing unit being capable of executing instructions to perform scalar data processing;

e) a vector processing unit [104] coupled to the chip interconnect [44] , the vector processing unit being capable of executing instructions to perform vector data processing; and

f) an input and output (see interface connections 22, 50,52 in fig.1)) interface coupled to the chip interconnect, the V0 interface receiving/transmitting data from/to the scalar and/or vector processing units.

4. As to the language of "chip interconnect", Beard did not explicitly characterize his system as chip interconnect as claimed. However, since Beard is directed to the interconnection of the integrated circuits ( fig.1), and since no specific type of chip interconnect has been reflected into the claim, it is read as any general integrated circuit input and output connecting on the arbitration node (switch) . The examiner holds that chip connection in general would not have been strange to Beard unless the chip connection had a special structure itself.

5. Beard did not specifically teach his memory controller including a DRAM as claimed. However, So taught a host system including a DRAM (see fig.22 DRAM [2255] ). It would have been obvious to one ordinary skill in the art to use So in Beard for including the DRAM as claimed because the use of So could provide Beard the capability to accept the data stream based on the dynamic access of a given cycle, and therefore, increasing the adaptability of the storage read and write control, and because So also taught his system could be programmed as scalar and vector (see col.20, lines 32-37), which was a suggestion of the applicability of the DRAM, as taught by So, into a scalar/vector system , such as taught by Beard, in order to enhance the storage capability, and for above reasons, provided a motivation.

6. As to claim 2, Beard also included a switch mechanism (see arbitration 44 in fig.1) coupled the chip interconnect and coupled to the scalar processing unit and coupled to the vector processing unit, the switch mechanism operable to receive multiple media data stream from the 1/0 interface and dispatch the multiple media data stream to the scalar processing unit and/or the vector processing unit .

7. As to claim 3, Beard also taught :

a) multiple scalar processing units, the multiple scalar processing units being capable of executing instructions to perform scalar processing simultaneously; and multiple vector processing units, the multiple vector processing units being capable of executing instructions to perform vector processing simultaneously (see the simultaneous operation by vector and scalar units in col.5, lines 51-68, col.6, lines 1-6, see the vector units 106 and scalar units 106 operate concurrently in col.6, lines 1-3) .

8. As to claim 4, Beard also taught multiple scalar processing units of a kind and multiple vector processing unit of a kind (see fig.2 for scalar, see fig.6 for vector).

9. As to claim 5, Beard also taught :

a) a general purpose register (GPR) file coupled to the scalar processing unit (see scalar registers 204 in fig.2);

b) a vector register (VR) file coupled to the vector processing unit (see vector registers in fig.3);

c) a special purpose register (see fig.1 L registers ) coupled to the chip interconnect; and a load and store unit (LSU), the LSU being capable of executing instructions to load and store scalar data from and to the GPR, and the LSU being capable of

executing instructions to load and store vector data from and to the VR (see fig.17, load request and store request, see also col.30, lines 65-67).

10. As to claim 6, Beard taught : loads and stores data from and to the memory location (see memory locating in fig.17).

11. As to claim 7, So also included a DMA (see col.116, lines 54-58).

12. As to claim 8, Beard also included bit length up to 32 (see col.7, lines 60-65).

13. As to claim 9, Beard also included dispatching of instruction simultaneously (see col.29, lines 57-60).

14. As to claim 10, SO also included VLIW (see col.15, lines 59-60).

15. As to claim 11 Beard also included :

a) a program counter;

b) a branch unit, wherein the program counter and the branch unit determine the location to fetch next instructions (see fig.1 branch unit);

c) an instruction cache memory (see instruction cache in fig.2), the instruction cache memory comprising instruction cache tag and data memories for buffering instructions transmitted from the host memory; and

d) at least one memory mapped registers accessible by the host (see memory map in fig.17).

16. As to claims 12,13, Beard also included :

a) an integer arithmetic and logic unit (see INT ADD Shift in fig.2) being capable of executing instructions to perform simple scalar integer arithmetic and logical operations;

b) an integer shift unit (see Integer Add Shift in fig2) being capable of executing instructions to perform scalar bit shifting and rotating operations; and

c) a floating point unit (See floating point add in fig.2), the FPU being capable of executing instructions to perform high precision scalar data processing.

17. As to claims 19,20, Beard's scalar data processing and vector data processing are performed autonomously and asynchronously to the host processor (see the separate control for the scalar and vector processing in col.6, lines 20-31) . Beard also included an interrupt mechanism (see interrupt mechanism in fig.1).

18. As to claim 21, Beard also included a set of memory mapped addresses (see fig.17).

19. As to claim 22, Beard was also applicable as stand alone because the vector processor can be implemented as single processor and did not need both the scalar and the vector (see col.5, lines 30-34).

20. As to claim 23, Beard also included a special purpose register (see control C registers in col.5, lines 45-50).

21. Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beard (5,430,884) in view of SO in view of Dowling (6,597,745).

22. As to claim 14, Beard did not specifically show the vector permutation, or the complex integer as clamed. However, Dowling taught system including a vector permutation (see col.13, lines 55-62) and complex integer (see complex integer in col.4, lines 1-8 ). It would have been obvious to one of ordinary skill in the art to use Dowling in Beard for including the vector permutation and complex integer as claimed because the sue of Dowling could provide Beard the ability to accept more complex data calculation (e.g. vector permuting and integer addition with multiply etc.), thereby expanding the processing capability of Beard, and because Beard did disclose a multiplicity of add , shit and logical units (see col.9, lines 25-47), which was a suggestion of the need for including the vector permutation complex integer for minimizing eh pipeline gaps, for the above reason , provide a motivation.

23. As to claim 15, Beard also disclosed a floating point unit (See floating point add in fig.2), the FPU being capable of executing instructions to perform high precision scalar data processing.

24. As to claim 16, SO disclosed a lookup (see fig.24A) and dma (col.116, lines 54-58).

25. As to claims 17, 18, SO disclosed DRAM and SRANM (see fig.22 DRAM [2255], see SRAM in SRAM in fig.51A ).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

26. Claims 24, 25, 26, 27, 28, 29, 30, 31, 33, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 49, 53,54,55,56,57,58,59,60,61,62,63,65,69,70,71 are rejected under 35 U.S.C. 102(b) as being anticipated by Beard (5,430,884).

27. As to claims 24,40,56, Beard taught a method, in an integrated circuit (IC) having a chip interconnect [44], and at least one host processor and a host memory [main memory] (see fig.1, the method comprising:

a) receiving data stream from an input/output interface (see interface from 22, 50 or 52 )coupled to the chip interconnect [memory arbitration node] (see ;

b) examining the data to determine whether the data require scalar data processing or vector data processing (see the col.1, lines );

c)performing scalar data processing on the data in the IC, if the data require scalar data processing (see the scalar processor port in fig.2) ; and

d) performing vector data processing on the data in the IC, if the data require vector data processing (see the vector data ports in fig.2, see also the vector processing data path in fig.6).

28. As to claims 25,41,57 , Beard also taught at least :

a) a scalar processing unit (see fig.2 scalar processor ) coupled to the chip interconnect [44], the scalar processing unit performing scalar data processing on the data; and

b) a vector processing unit (see fig.2 vector processor) coupled to the chip interconnect [44] , the vector processing unit performing vector data processing on the data.

29. As to claims 26,42,58, Beard also taught multiple scalar processing units performing scalar data processing simultaneously and multiple vector processing units performing vector data processing simultaneously (se the simultaneous operation by vector and scalar units in col.5, lines 51-68, col.6, lines 1-6, see the vector units 106 and scalar units 106 operated concurrently in col.6, lines 1-3).

30. As to claim 27,43, 59, Beard also taught :

a) dispatching the data to the scalar processing unit if the data require scalar data processing (see the data path to the scalar processor in fig.2); and

b) dispatching the data to the vector processing unit if the data require vector data (see the data path and write port in vector processor in fig.2,and fig.6) .

31. As to claim 28, 44,60, Beard also taught the switch mechanism receiving the data from the I/O interface (see interface 22 and 50 and 52).

32. As to claims 29, 45,61, Beard also included an instruction unit capable of decoding the data (see instruction unit in fig.2).

33. As to claim 30, 46,62, Beard also included :

a) a general purpose register (GPR) file coupled to the scalar processing unit (see scalar registers 204 in fig.2);

b) a vector register (VR) file coupled to the vector processing unit (see vector registers in fig.3);

c) a special purpose register (see fig.1 L registers ) coupled to the chip interconnect; and a load and store unit (LSU), the LSU being capable of executing instructions to load and store scalar data from and to the GPR, and the LSU being capable of executing instructions to load and store vector data from and to the VR (see fig.17, load request and store request).

34. As to claims 31,47, 63, Beard taught a memory location coupled to the chip Interconnect [44] , wherein the LSU loads and stores data from and to the memory location (see memory locating in fig.17, col.30, lines 65-67).

As to claims 33, 49, 65, Beard also taught :

a) an integer arithmetic and logic unit (see INT ADD Shift in fig.2) being capable of executing instructions to perform simple scalar integer arithmetic and logical operations;

b) an integer shift unit (see Integer Add Shift in fig2) being capable of executing instructions to perform scalar bit shifting and rotating operations; and

c) a floating point unit (See floating point add in fig.2), the FPU being capable of executing instructions to perform high precision scalar data processing.

35. As to claims 37, 53,69, Beard's scalar data processing and vector data processing are performed autonomously and asynchronously to the host processor (see the separate control for the scalar and vector processing in col.6, lines 20-31) .

36. As to claims 38, 54,70, Beard also included an interrupt mechanism (see interrupt mechanism in fig.1).

37. As to claims 39,55,71, Beard also included a set of memory mapped addresses (see fig.17).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

38. Claims 32, 48, 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beard (5,430,884) in view of So (5,909,559).

39. As to claims 32,48,64, Beard did not specifically teach the DMA access to host as clamed. However, So taught a host access through a direct memory (DMA) operation (see col.116, lines 54-58). It would have been obvious ton e of ordinary skill in the art to sue So in Beard for including the DMA as claimed because the use Of So could provide Beard the ability to access the host memory directly without the causing

the delay time in to the processor, and it could achieved by configuring the DMA of So into Beard with modified system parameters (e.g. the R/W ports) so that the specific DMA access of So could be recognized by Beard, and because Beard did taught his system was directed to scalar/vector processor was used for maximizing the pipelined performance (see col.3, lines 16-26), which was an indicating of the need for providing memory direct access , such as DMA, in order to minimize the latency of the processor, and therefore, to enhanced overall performance, and for doing so, provided a motivation.

40. Claims 34,50 , 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beard (5,430,884) in view of Dowling (6,597,745).

41. As to claims 34,50,66, Beard did not specifically show the vector permutation, or the complex integer as clamed. However, Dowling taught system including a vector permutation (see col.13, lines 55-62) and complex integer (see complex integer in col.4, lines 1-8 ). It would have been obvious to one of ordinary skill in the art to use Dowling in Beard for including the vector permutation and complex integer as claimed because the sue of Dowling could provide Beard the ability to accept more complex data calculation (e.g. vector permuting and integer addition with multiply etc.), thereby expanding the processing capability of Beard, and because Beard did disclose a multiplicity of add , shit and logical units (see col.9, lines 25-47), which was a

suggestion of the need for including the vector permutation complex integer for minimizing eh pipeline gaps, for the above reason , provide a motivation.

42. Claims 35,36, 51,52, 67,68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beard (5,430,884) in view of Dowling (6,597,745) as applied to claim 34 above, and further in view of SO (5,909,559).

43. As to claims 35,36, neither Beard nor Dowling specifically showed the lookup , nor the DMA as claimed. However, SO disclosed a lookup (see fig.24A) and dma (col.116, lines 54-58). It would have been obvious to one of ordinary skill in the art to use lookup and DMA because the use of SO could provide reduced processing cycle of the scalar/vector in Beard by the access the lookup or DMA directly without the causing the overheads unto the processor, and since no specific format of the lookup and DMA has been reflected into the clam, one of ordinary skill in the art should be able to recognize the advantages of using the lookup and dma into Beard in order to provide the minimized processing overheads of the processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***21 Century Strategic Plan***

DANIEL H. PAN
PRIMARY EXAMINER
GROUP